TITLE

METHOD FOR FABRICATING COPPER INTERCONNECTS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor fabrication, and in particular to methods for capping copper interconnects in semiconductor devices.

Description of the Related Art

Conventional semiconductor devices comprise conductive interconnects to establish electric contact with conductive structures inside semiconductor substrates. Interconnects comprise metal lines and metal plugs formed in dielectric layers for horizontal and vertical connections.

High performance semiconductor applications require rapid speed in semiconductor circuitry. The speed of semiconductor circuitry varies inversely with the resistance and capacitance of the interconnection pattern. As integrated circuits become more complex and feature size and space become smaller, the integrated circuit speed becomes more dependent upon the interconnect pattern, and thus, materials utilized in interconnect structures have become a major concern.

One approach to increase the control speed of semiconductor circuitry is to reduce the resistance of interconnects. Cu and Cu alloys are utilized as a better material for replacing Al in VLSI interconnect metallization. Cu exhibits superior electromigration properties and has a lower resistivity than Al. In addition, copper or copper alloy interconnects can be formed by electroless plating and electroplating, which is low cost, has high throughput, high quality, is highly efficient and has good filling capabilities.

Although Cu or Cu alloy interconnects have superior properties for applications, there are drawbacks in Cu implementation. For example, Cu readily diffuses into dielectric layers, particularly silicon dioxide, which results in electrical shorts.

A well-known solution to prevent Cu diffusion is to form diffusion barrier layers between Cu or Cu alloy interconnects and dielectric layers. Conventional diffusion barrier layers include tantalum (Ta)/tantalum nitride (TaN), titanium nitride (TiN), titanium-tungsten (TiW), tungsten (W)/tungsten nitride (WN) for encapsulating Cu interconnects. The diffusion barrier layers are usually deposited on bottoms and sidewalls of damascene openings by sputtering before Cu filling. The surface of exposed Cu or Cu alloy interconnects after planarization are conventionally capped by silicon nitride.

The drawback of silicon nitride is poor adhesion to copper. The subsequent process usually causes silicon nitride to peel away from the copper plugs. The peeled silicon nitride creates a path for copper to diffuse outward and for moisture or contaminates to diffuse inward and thus degrade reliability of the interconnects.

In U.S. Pat. No. 5,447,887, the adhesion problem of a silicon nitride capping layer to a copper interconnect is addressed by initially treating the exposed surface with silane in the absence of a plasma to form a thin layer of copper silicide, and depositing a silicon nitride capping layer thereon.

U.S. Pat. No. 6,492,266 discloses enhancing the adhesion of a diffusion barrier or capping layer to a Cu or Cu alloy interconnect member by treating the exposed surface of the Cu or Cu alloy interconnect member: (a) under plasma conditions with ammonia and silane or dichlorosilane to form a copper silicide layer thereon; or (b) with an ammonia plasma followed by reaction with silane or dichlorosilane to form a copper silicide layer thereon.

U.S. Pat. No. 6,339,025 discloses fabricating a copper capping layer by forming a silicon rich nitride layer on an exposed copper layer. The silicon in the silicon rich nitride layer easily reacts with the copper and a copper silicide layer is formed between the copper and the silicon rich nitride layer.

SUMMARY OF THE INVENTION

The present invention provides methods to form copper silicide as a capping layer of copper interconnects.

In one embodiment, a dielectric layer is formed overlaying a semiconductor substrate. An opening is formed in the dielectric layer and subsequently embedded copper or copper alloy to form a interconnect structure. A silicon layer is formed on

the copper or copper alloy by sputtering or chemical vapor deposition. A copper silicide layer is formed by reacting the silicon layer with the underlying copper or copper alloy as a capping layer.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

Figs. 1A to 1G are cross-sections illustrating fabrication of a copper silicide layer capping on a copper interconnect.

DETAILED DESCRIPTION OF THE INVENTION

In Fig. 1A, a semiconductor substrate 100 is provided with a conductive structure 102 thereon, such as a gate electrode or a metal line. A dielectric layer 110 is deposited overlying the semiconductor substrate 100. The preferred dielectric layer 110 is low-k material ($k \leq 3.2$), such as organic low-k material, CVD low-k material, or a combination thereof. The dielectric layer can also be fluorinated silica glass (FSG), SiC, SiOC, SiOCN, carbon-containing silicon oxide or nitrogen-containing silicon oxide.

A damascene opening 120 is subsequently formed within the dielectric layer 110 to expose the underlying conductive structure 102 as shown in FIG. 1B. The preferred width of the opening 120 is less than 900Å. Preferably, the opening 120 is defined by a conventional dual damascene process to form a trench and a via opening.

The opening 120 is filled with copper or copper alloy to form a copper plug 130, as Fig. 1C shows. In one embodiment, a diffusion barrier layer (not shown), e.g. TaN, TiN or TiW, is formed on the bottom and sidewall of the opening 120 by sputtering to block cupper diffusion into the dielectric layer. A copper seed layer (not shown) is subsequently formed on the opening 120, and then copper or copper alloy is embedded into the opening 120 by electro-chemical plating or electroless plating. In another embodiment, the opening 120 is filled with copper or copper alloy by

chemical vapor deposition (CVD). The extra copper or copper alloy over the dielectric layer 110 is removed by planarization, such as by chemical mechanical polishing, to form a copper plug 130 as Fig. 1C shows. The preferred thickness of the copper or copper alloy plug 130 is less than 4000Å.

A silicon layer 140 is formed overlying the surface of the copper plug 130 and the dielectric layer 110 as shown in Fig. 1D. In a preferred embodiment, an amorphous silicon layer is deposited on the surface of the substrate 110 by sputtering, wherein the substrate 110 is attached to one electrode, and a target of silicon is placed on a second electrode. These electrodes are connected to a high voltage power supply and a gas which is usually a mixture of argon, and hydrogen is introduced between the electrodes to provide a medium in which a glow discharge or plasma can be initiated and maintained. The glow discharge provides ions that strike the silicon target, causing removal by momentum transfer of the mainly neutral target atoms, which subsequently condense as a thin film on the substrate electrode. Also, the glow discharge functions to activate the hydrogen causing it to react with the silicon, and be incorporated into the deposited silicon film. The activated hydrogen also coordinates with the dangling bonds of the silicon to form mono, di, and trihydrides.

In another preferred embodiment, amorphous silicon layer 140 is formed by chemical vapor deposition (CVD), such as plasma-enhanced CVD (PECVD) with silane gas at 200 to 450 degrees C. The preferred thickness of the amorphous silicon layer 140 is about 50Å to 500Å.

The semiconductor substrate 110 is then subjected to an inert gas-containing ambience at a temperature of about 150 degrees C. to about 450 degrees C. to form a copper silicide layer ($CuSi_X$) 142 between the surface of the copper plug 130 and the above amorphous silicon layer 140, as shown in Fig. 1E. Preferably, the substrate 110 is subjected in a furnace or a rapid thermal annealing (RTA) chamber for copper silicide formation.

The un-reacted silicon layer 140 is then removed to expose the dielectric layer 110, as Fig. 1F shows. The copper silicide 142 serves as a capping layer of copper interconnects, which improves the adhesion between the copper or copper alloy plug 130 and above layers. Thus, the capped copper silicide layer 142 will not peel in the subsequent process and consequently improves the reliability of the semiconductor device.

In Fig. 1G, a diffusion barrier layer 150 is preferably deposited on the surface of the substrate 110 by PECVD with a thickness of 200Å to 2000Å, covering the copper silicide layer 142 and the dielectric layer 110. The diffusion barrier layer 150 can be SiN, SiC, SiOC, SiOCN, silicon-rich oxide, carbon-containing silicon oxide, nitrogen-containing silicon oxide, or a combination thereof. An etch-stop layer 160 is optionally formed on the diffusion barrier layer 150 by PECVD at 300 degrees C to 450 degrees C., which can be SiN, SiC, SiOC, and SiOCN, silicon-rich oxide, carbon-containing silicon oxide or nitrogen-containing silicon oxide. The etch-stop layer 160 serves as a stop layer for subsequent interconnect processes.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.